2021_10_28 - LG

Updated with schedule and milestones

From: EICSC

eRD104 FY2022 work plan proposal

In FY22 the eRD104 and eRD111 efforts will concentrate on R&D and prototyping in the areas described below.

eRD104 Silicon Services Reduction

Services Reduction

Silicon tracking detector services reduction efforts are concentrated in the areas where the bulk of the detector services exists. Specifically in the powering system and the readout system. While the specifics of the R&D and prototyping in this proposal will be formulated for the silicon tracking powering and readout systems, we welcome working with other detector subsystems on services reductions in these areas. Commonality of components over detector subsystems is a useful attribute.

Powering system

By far the largest component of services for the silicon tracking detector in traditional (ALICE ITS2 like [1]) configurations is the powering system cabling. The goal of this R&D is to investigate the possibilities of serial powering, possibly with on-chip regulation and/or the use of on detector radiation tolerant DC-DC converters. These powering system architectures could reduce the material from power cables substantially. Some preliminary work has already been done in this area [2], but it needs to be expanded and extended.

Readout system

The readout cabling for the silicon tracking detector, currently projected to consist of samtec twinax, also is a significant fraction of the servicing load required for the detector. In this R&D topic we will investigate the use cases and possible topologies and technological solutions for a multiplexing system based on radiation tolerant FPGAs to aggregate the data from the sensor outputs and transmit this aggregated data outside of the detector volume on high speed optical links.

Budget and milestones

Please note that the budget given below is described in the US DOE system where scientific staff already on grant (staff, postdoc) are not costed to the project but support staff (engineers, technicians, etc.) are costed to the project. The nature of international collaborations invite the possibility that some of this work will be done in institutions that adhere to different funding systems. As such, the numbers presented represent the high limit expected to do the tasks described.

Silicon	Mechanical	Electrical	Mechanical	Electrical	postdoc (h)	staff (h)	student	materials (k$)	total (k$)

	Designer (h)	Engineer (h)	Engineer (h)	Technician (h)	Technician (h)			(h)		
Services Reduction		0.0	144.0	0.0	60.0	0.0	123.0	72.0	5.4	36.2
total with overhead										47.0

These budget numbers assume labor rates consistent with LBNL labor rates (staff and postdoc are not costed as part of the totals presented here) and an overhead of 30% (to be checked).

Note that the UK contribution is in-kind as it is funded via the UKRI-STFC Infrastructure Bid for EIC R&D.

Milestones

The following milestones are anticipated and shown in the schedule flow..

Milestone Description	**Date**
report on serial powering	2022/04/29
report on DC-DC powering	2022/06/24
FY22 assessment report on powering options	2022/09/29
erd104 FY22 report	2022/09/30

Services Reduction Deliverables

FY22 services reduction deliverables will include:

1. Build upon the initial assessment of possible benefits of serial/DC-DC converters powering schemes and detail possible configurations with analysis of architectural benefits/weaknesses and assessment of current and upcoming DC-DC converter candidates in written report form.
2. Single branch construction, testing and characterization of existing DC-DC converter candidates in likely architectures with written report. This work can be extended to other detector configurations/needs with appropriate consultation and architectures/requirements.
3. Research into existing serial powering schemes used by ATLAS and other experiments with analysis and extrapolation into EIC case.
4. If feasible, get example hardware and characterize. Otherwise examine on-chip or hybridized regulators.

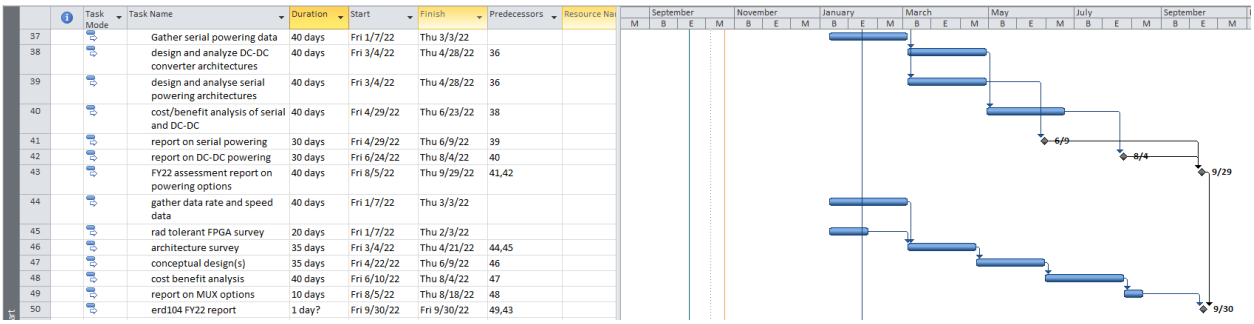
5. Examination of capabilities of components needed for multiplexing (rad-hard FPGAs and optical modules) and preliminary studies of the tradeoffs in architectural approaches.
6. Written progress report.

Labor Force

EICSC members will provide the labor force for the above proposed FY22 activity. The breakdown of EICSC institutions involved and a contact persons for the activities is shown in the following table. Please note that the effort table is not yet complete, more institutions will be joining the topics shown and this table will continue to be updated.

Topic	**Institutions involved**	**Contact Person**
Powering System	University of Birmingham, STFC RAL PPD	Laura Gonella (Univ of Birmingham), Fergus Wilson (RAL)
Readout system	ORNL, BNL	Jo Schambach (ORNL)

Schedule



	Task Mode	Task Name	Duration	Start	Finish	Predecessors	Resource Na
37		Gather serial powering data	40 days	Fri 1/7/22	Thu 3/3/22		
38		design and analyze DC-DC converter architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
39		design and analyse serial powering architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
40		cost/benefit analysis of serial and DC-DC	40 days	Fri 4/29/22	Thu 6/23/22	38	
41		report on serial powering	30 days	Fri 4/29/22	Thu 6/9/22	39	
42		report on DC-DC powering	30 days	Fri 6/24/22	Thu 8/4/22	40	
43		FY22 assessment report on powering options	40 days	Fri 8/5/22	Thu 9/29/22	41,42	
44		gather data rate and speed data	40 days	Fri 1/7/22	Thu 3/3/22		
45		rad tolerant FPGA survey	20 days	Fri 1/7/22	Thu 2/3/22		
46		architecture survey	35 days	Fri 3/4/22	Thu 4/21/22	44,45	
47		conceptual design(s)	35 days	Fri 4/22/22	Thu 6/9/22	46	
48		cost benefit analysis	40 days	Fri 6/10/22	Thu 8/4/22	47	
49		report on MUX options	10 days	Fri 8/5/22	Thu 8/18/22	48	
50		erd104 FY22 report	1 day?	Fri 9/30/22	Fri 9/30/22	49,43	

References

[1] B. Abelev et al., Technical Design Report for the Upgrade of the ALICE Inner Tracking System, J. Phys. G 41 (2014) 087002, doi:10.1088/0954-3899/41/8/087002.

[2] A. Collu, L. Greiner, Powering options for an EIC silicon tracker https://www.eicug.org/web/sites/default/files/Powering-options-for-an-EIC-silicon-tracker.pdf